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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/542,783	04/04/2000	John Whitman	4294US(98-1208)	6870

7590 10/31/2006

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/542,783	WHITMAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) *18-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicants' submission filed on September 25, 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-9, 11, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Yoshihara (US/6,117,486).

Re claims l and 3-7, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (20) on at least a portion of the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of said at least one recess (23a) without subsequently removing the material (20) from the surface, an upper surface said material (20) being appear substantially planar (23 24 25 26) (see Figs. 6A-6D; 10A-10E and 13A-13E;).

However, Kikuchi et al. do not specifically disclose with certainty the upper surface portion of the material within the recess substantially planar.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the

method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness (i.e., it is analogous to substantially planar).

Re claim 2, as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including disposing the material so as to substantially fill the at least one recess without substantially covering said surface (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 8, as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess (see Figs. 6A-6D; 10A-10E and 13A-13E).

Re claim 9, as applied to claim 1 above, Kikuchi et al. Yoshihara in combination disclose all the claimed limitations including the limitation wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material (see Figs. 6A-6D; 10A-10E; 13A-13E)

Re claim 11 as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said semiconductor device structure (see Fig. 6A-6D; 10A-10E; 13A-13E).

Re claims 16 and 17, as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including the limitation providing a

semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material, with a non-planar surface disposed in said at least one dual damascene trench add at least partially covering sand surface and disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing (see Figs. 14A-14D).

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) and Yoshihara (US/6,117,486), as applied in Paragraph 3 above, and further in view of Lin et al. (US/6,046,083).

Re claim 10, as applied to claim 9 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including forming of stacked capacitor structure having conductive layer. Although it is well-known in the art Kikuchi et al. do not disclose doped HSG.

Lin et al. disclose providing said semiconductor device structure having a stacked capacitor structure with the surface and at least one container being lined, with doped hemispherical grain polysilicon (see Figs. 7 and 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. and Yoshihara in reference with doped HSG as taught by Lin et al. because the device performance would have been enhanced (see Lin et al. Col. 1, lines 59-67 through Col. 2, lines 1-14).

5. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153), and Yoshihara (US/6,117,486), as applied in Paragraph 3 above, and further in view of Park et al. (US/6,326,282).

Re claim 12, as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including the limitation except providing a shallow trench

isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

Park et al. disclose forming of a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure in order to form an isolation region between the device elements (see Figs. 2B-2E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. and Yoshihara reference with shallow trench isolation structure as taught by Park et al. because the shallow trench isolation structure would have provided isolation region between device elements in the substrate.

Re claim 13, as applied to claim 12 above, Kikuchi et al., Yoshihara and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said shallow trench isolation structure (see Park et al. Figs. 2B-2E).

Re claim 14, as applied to claim 12 above, both Kikuchi et al., Yoshihara and Park et al. in combination disclose all the claimed limitations including the limitation wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface see Park et al. Figs. 2B-2E).

Re claim 15, as applied to claim 14 above, both Kikuchi et al., Yoshihara and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress

buffer having a substantially planar surface without removing material thereof following said disposing see Park et al. Figs. 2B-2E).

Response to Arguments

6. Applicants' arguments filed on September 25, 2006 have been fully considered but they are not persuasive.

The instant application is rejected in view of the Board's decision of July 25, 2006. As stated by the Board, the rejection of claim 1 under 35 U.S.C. 103 is deemed proper because the prior art of record provides sufficient evidence for the planar surface. (see Board's new ground of rejection of claim 1 in Page 12). In addition, the rejection of claims 2 and 8-17 is also consistent with the Board's recommendation based upon the examiner's determination of the prior art of record. After further consideration, as directed by the Board, there is sufficient evidence and teaching in the record that the combination of Kikuchi et al. '153 and Yoshihara '486 is provided planar surface and the rejection of claims 2 and 8-17 is deemed proper because the rejection of claim 1 is deemed proper as the Board determined.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

7. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1950.

Brook Kebede
Primary Examiner
Art Unit 2823

BK
October 29, 2006